Attorney Docket No.: SAM-167

TRENCH ISOLATION METHOD

This application relies for priority upon Korean Patent Application No. 2000-39317, filed on July 10, 2000, the contents of which are herein incorporated by reference in their entirety.

Field of the Invention

The present invention relates to a method of manufacturing a semiconductor device and, more particularly, to a trench isolation method for manufacture of a semiconductor device.

Background of the Invention

A device isolation layer is formed on a semiconductor substrate in order to define active regions and electrically isolate the active regions from each other. As a method of forming the device isolation layer, local oxidation of silicon (LOCOS) technique and trench isolation technique are commonly utilized. Since a semiconductor substrate is locally subject to thermal oxidation to form a field oxide layer, LOCOS is a relatively simple process. As the integration level of semiconductor devices increases, an abnormal feature on the oxide layer referred to as a "bird's beak" or poor planarity caused by the LOCOS process have become serious problems. Accordingly, the trench isolation technique has widely been utilized.

In the trench isolation technique, an etching mask for a trench is formed on a semiconductor substrate. Using the etching mask, the semiconductor substrate is etched to form a trench, which is then filled with an insulating layer. In the following wet

etching process, the insulating layer is etched, which could cause a deterioration of the characteristics of the device isolation layer. Accordingly, the insulating layer is densified for preventing the deterioration. The densification is carried out by annealing the insulating layer in oxygen ambient at a temperature of 900°C~1200°C for an hour.

Since the densification is carried out at a high temperature, this changes the volumes an insulating layer formed in a trench and a semiconductor substrate vary. The thermal expansion ratio of the insulating layer is different from that of the semiconductor substrate, so that stress is applied to the trench inner wall that serves as an interface therebetween.

U. S. Patent No. 6,037,237 discloses a method of forming an insulating layer composed of stacked layers whose stress characteristics are different from each other when the insulating layer is formed to fill a trench. According to this approach, an insulating layer having a compressive stress characteristic, and an insulating layer having a tensile stress characteristic, for example, a USG (undoped silicate glass) layer and a PTEOS (plasma tetraethylorthosilicate) layer, or an HDP (high density plasma) layer and the PTEOS layer, are stacked to reduce stress applied to the semiconductor substrate during the densification. An upper insulating layer is made of an insulator of favorable planarization characteristic, easily carrying out the following planarization etching process.

Although the insulating layer of a stack structure is formed for reducing the stress, the following densification still puts a burden on the overall process. That is, stress created in the high thermal annealing process cannot entirely be removed, and therefore causes a declination in productivity.

Summary of the Invention

Therefore, it is an object of the present invention to provide a trench isolation method which avods the need for a densification process for densifying the insulating layer formed in the trench.

According to an aspect of the present invention, a pad oxide layer and etch-stop layer are sequentially formed on a semiconductor substrate. With a patterning process, the etch-stop layer and the pad oxide layer are sequentially etched to form an etching mask pattern that exposes a predetermined region of the semiconductor substrate. Using the etching mask pattern as an etching mask, the exposed semiconductor substrate is etched to form a trench. An oxide layer is formed on an inner wall and a bottom of the trench, and then an oxidation barrier layer is formed on the oxide layer. An insulating layer to fill the trench is formed on an overall surface of the above resulting structure where the oxidation barrier layer is formed. Using a layer formed at a high temperature, a material layer is formed on the insulating layer. During formation of the material layer, the insulating layer is densified. The material layer is made of one selected from a group consisting of, for example, HTO (high temperature oxide), high temperature USG (undoped silicate glass), polysilicon, and amorphous silicon that are formed at a temperature of 500°C and higher. The material layer and the insulating layer are planarly etched down to a top surface of the etching mask pattern, so that a device isolation layer is formed. Then, the exposed etching mask pattern is removed to form a trench isolation layer.

Brief Description of the Drawings

A further understanding of the nature and advantage of the invention herein may be realized by reference to the remaining portions of the specification and the attached drawings.

Fig. 1A through Fig. 1H are cross-sectional views for description of a trench isolation method in accordance with the present invention; and

Fig. 2A and Fig. 2B are scanning electron microscope (SEM) photos showing a profile of a trench isolation layer in accordance with a prior art and the present invention, respectively.

Detailed Description of Preferred Embodiments

Referring to Fig. 1A, a pad oxide layer 12 is formed on an overall surface of a semiconductor substrate 10. An etch-stop layer 13 is formed on the pad oxide layer 12. The pad oxide layer 12 serves as a buffer layer for reducing stress applied to the substrate 10, and the etch-stop layer 13 is used as an etching mask in the following process for forming a trench. The pad oxide layer 12 is comprised of, for example, thermal oxide, having a thickness of 20Å~200Å. The etch-stop layer 13 comprises, for example, silicon nitride or polysilicon. If the etch-stop layer 13 is made of polysilicon, it is preferable that an HTO layer (not shown) is additionally formed on the polysilicon layer. This additional layer removed the need for etching the polysilicon layer in the following process for forming a trench.

Referring to Fig. 1B and Fig. 1C, a photoresist layer is formed on the etch-stop layer 13. The photoresist layer is patterned to form a photoresist pattern 15 to define a trench region. Using the photoresist pattern 15 as an etching mask, the etch-stop layer 13 and the pad oxide layer are sequentially etched to expose a predetermined region of the substrate 10. An etching mask pattern is then formed, which is composed of a pad oxide

layer pattern 12a and an etch-stop layer pattern 13a stacked sequentially. With O_2 plasma ashing, the photoresist pattern 15 is removed.

Referring to Fig. 1D and Fig. 1E, using the etching mask pattern 16 as an etching mask, the exposed substrate 10 is dry etched to form a trench 17. In order to cure etching damage applied to the substrate 10 in forming the trench 17, an oxide layer 19 is formed on an inner wall and a bottom of the trench 17. The oxide layer 19 is made of, for example, thermal oxide or chemical vapor deposition (CVD) oxide with a thickness of 20Å~200Å. If the CVD oxide layer is formed, an annealing process is then carried out.

In order to prevent the inner wall of the trench 17 from additionally being oxidized, a silicon oxide layer, i.e., oxidation barrier layer 20 is formed on an overall surface of the resulting structure where the oxide layer 19 is formed. It is preferable that a capping layer 21, for example, CVD oxide layer for protecting the oxidation barrier layer 20, is formed on the oxidation barrier layer 20. The capping layer 21 prevents damage of the oxidation barrier layer 20 in the following process for forming an insulating layer which fills a trench. Specifically, if the trench is filled with an HDP oxide layer, the capping layer 21 protects the oxidation barrier layer 20 from etching with argon. If the trench is filled with a USG layer instead of the HDP oxide layer, on an overall surface of the above resulting structure where the trench 17 is formed, plasma treatment is carried out to improve deposition characteristic of the USG layer. In this case, the oxidation barrier layer 20 may be damaged from plasma. The capping layer 21 prevents the damage of the oxidation barrier layer 20. The oxidation barrier layer 20 and capping layer 21 are formed to have a thickness of 20Å~300Å, respectively.

Referring to Fig. 1F, on an overall surface of the above resulting structure where the capping layer 21 is formed, an insulating layer 23 is formed to fill the trench 17. The

insulating layer 23 comprises, for example, HDP oxide or USG whose gap-filling characteristics are such that the trench can be filled without void.

As a feature of the present invention, a material layer 24 is then formed on the insulating layer 23. The material layer 24 comprises a material whose planarization characteristic is such that the following polarization etching process can easily be carried out. It is preferable that the material layer 24 comprises material having stress characteristics which can reduce stress applied to the semiconductor substrate 10 by the insulating layer 23. Further, the material 24 is deposited at a temperature high enough to densify the insulating layer 23, preferably, at a temperature of 500˚C and higher. Since therefore the insulating layer 23 is densified while forming the material layer 24, a subsequent densification process can be avoided.

The material layer 24 may comprises, for example, a material selected from a group consisting of, for example, HTO, high temperature USG, polysilicon, and amorphous silicon. Specifically, the HTO layer is formed by a CVD process using SiH_4 gas and O_2 gas at a temperature of 700˚C~800˚C. The high temperature USG layer is formed by a CVD process using TEOS at a temperature of about 500˚C. The polysilicon layer is formed by a CVD process using SiH_4 gas at a temperature of 600˚C~700˚C. The amorphous silicon layer is formed by a CVD process using SiH_4 at a temperature of 500˚C~600˚C.

Referring to Fig. 1G, with a chemical mechanical polishing (CMP) process, the material layer 24 and the insulating layer 23 are planarly etched down to a top surface of the etching mask pattern 16. So a device isolation layer pattern 23a filling a trench is formed.

Referring to Fig. 1H, the etching mask pattern 16 is wet etched to complete a

device isolation 23b. If the etch-stop layer pattern 13a is made of silicon nitride, it is etched using phosphoric acid solution. The pad oxide layer 12a is etched using fluoric acid solution.

According to the method, the trench 17 is filled with the insulating layer 23, and then the insulating layer 23 is densified while depositing the material layer 24. Thus, it is possible to form a trench isolation layer 23b having a low wet etching rate without carrying out a densification process.

Fig. 2A is an SEM photo showing a profile of a trench isolation layer in accordance with a prior art. A trench is formed and annealed in oxygen ambient at a temperature of 850°C, so that a thermal oxide layer grows on an inner side and a bottom of the trench to a thickness of 110Å. With a CVD process, a nitride layer is formed on the thermal oxide layer to a thickness of 55Å. A CVD oxide layer is formed on the nitride layer to a thickness of 100Å. An HDP oxide layer is formed to a thickness of 5500Å to fill the trench. A PTEOS layer is formed on the HDP oxide layer to a thickness of 2000Å, and is annealed at a temperature of 1050°C for an hour. Thus, a densification process is completed.

Fig. 2B is an SEM photo showing a profile of a trench isolation layer in accordance with the present invention. With a method same as described in Fig. 2A, a thermal oxide layer, a nitride layer, and a CVD oxide layer are sequentially formed on an inner wall of a trench. An HDP oxide layer is then formed to a thickness of 5500Å to fill the trench. An HTO oxide layer is then formed on the HDP oxide layer at a temperature of 780°C.

As shown in Fig. 2A and Fig. 2B, a profile (see Fig. 2B) of a trench isolation

layer which does not undergo a densification process is nearly similar to a profile (see Fig. 2A) of a trench isolation layer which undergoes the densification process. That is, although the densification process is avoided, the present invention makes it possible to suppress excessive recess of an edge of a device isolation layer.

According to the present invention, a trench is filled with an insulating layer on which a material layer formed at a high temperature is stacked. The insulating layer is densified while forming the material layer, so that the densification process is not needed. Therefore, it is possible to simplify the process and enhance productivity.

Further, the present invention avoids the need for a densification process that anneals an overall surface of a semiconductor substrate at a high temperature. Therefore, stress applied to the substrate is reduced to improve reliability of devices.

In the drawings and specification, there have been disclosed typical preferred embodiments of the invention and, although specific terms are employed, they are used in a generic and descriptive sense only and not for purpose of limitation, the scope of the invention being set forth in the following claims.